

CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

- 1 1. A method of forming an asymmetric field effect
2 transistor to control floating body effect, said
3 method including steps of
4 defining a gate location with a trench in a
5 dielectric layer on a semiconductor layer,
6 supplying impurities to said semiconductor
7 layer at edges of said trench and adjacent source
8 and drain regions, and
9 forming a gate structure on said semiconductor
10 layer in said trench.
- 1 2. A method as recited in claim 1, including
2 further steps of
3 removing said dielectric layer, and
4 forming source and drain impurity regions
5 adjacent said gate structure.
- 1 3. A method as recited in claim 2, wherein said
2 step of forming source and drain impurity regions is
3 performed by impurity implantation.
- 1 4. A method as recited in claim 2, including a
2 further step of
3 depositing an insulator layer over said source
4 and drain regions and said gate structure.

- 1 5. A method as recited in claim 4, including a
2 further step of
3 planarizing said insulator layer to said gate
4 structure.
- 1 6. A method as recited in claim 1, wherein said
2 gate location is defined between source and drain
3 impurity regions.
- 1 7. A method as recited in claim 6, including a
2 further step of
3 planarizing said gate structure to said
4 dielectric layer.
- 1 8. A method as recited in claim 1, wherein said
2 step of supplying impurities is performed by angled
3 implantation within said trench.
- 1 9. A method as recited in claim 1, including the
2 further step of forming a sidewall within said
3 trench.
- 1 10. A method as recited in claim 1, wherein said
2 sidewall is a doped material and said step of
3 supplying impurities is performed by diffusion from
4 said sidewall.
- 1 11. A method as recited in claim 1, wherein said
2 semiconductor layer is formed on an insulator layer.

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1 12. An asymmetric field effect transistor formed by
2 a process including steps of
3 defining a gate location with a trench in a
4 dielectric layer on a semiconductor layer,
5 supplying impurities to said semiconductor
6 layer at edges of said trench and adjacent source
7 and drain regions, and
8 forming a gate structure on said semiconductor
9 layer in said trench.

1 13. A transistor as recited in claim 12, said
2 process including further steps of
3 removing said dielectric layer, and
4 forming source and drain impurity regions
5 adjacent said gate structure.

1 14. A transistor as recited in claim 13, wherein
2 said step of forming source and drain impurity
3 regions is performed by impurity implantation.

1 15. A transistor as recited in claim 13, said
2 process including a further step of
3 depositing an insulator layer over said source
4 and drain regions and said gate structure.

1 16. A transistor as recited in claim 15, said
2 process including a further step of
3 planarizing said insulator layer to said gate
4 structure.

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1 17. A transistor as recited in claim 12, wherein
2 said gate location is defined between source and
3 drain impurity regions.

1 18. A transistor as recited in claim 17, said
2 process including a further step of
3 planarizing said gate structure to said
4 dielectric layer.

1 19. A transistor as recited in claim 12, wherein
2 said step of supplying impurities is performed by
3 angled implantation within said trench.

1 20. A transistor as recited in claim 12, said
2 process including the further step of forming a
3 sidewall within said trench.

1 21. A transistor as recited in claim 12, wherein
2 said sidewall is a doped material and said step of
3 supplying impurities is performed by diffusion from
4 said sidewall.

1 22. A transistor as recited in claim 12, wherein
2 said semiconductor layer is formed on an insulator
3 layer.